# A back-illuminated global-shutter CMOS image sensor with pixel-parallel 14-bit subthreshold ADC

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**Abstract** This paper reports on a back-illuminated, global-shutter, CMOS image sensor with a pixel-parallel, single-slope analog-to-digital converter (ADC). We adopted a digital bucket relay transfer with a multistage flip-flop connection, a pixel unit Cu–Cu connection, and positive-feedback circuitry to realize a 6.9 μm × 6.9 μm, 1.46 MP pixel-parallel ADC. By operating the comparator with a bias current in the subthreshold region of 7.74-111 nA, we succeeded in reducing the peak current during the simultaneous analog-to-digital conversions. In combination with an ADC standby operation, we succeeded in further reducing the pixel-parallel ADC power consumption. With these techniques, we realized a normalized index of figure-of-merit of 0.24 nJ·e-rms/step, which was calculated by dividing the entire sensor power by the effective ADC resolution at a subthreshold current of 111 nA during 660 fps operation.

**Keywords:** CMOS image sensors, imagers, global shutter, analog-to-digital conversion, subthreshold current, stacking, back illumination, Cu–Cu connection, in-pixel analog-to-digital conversion

## 1. Introduction

Rolling shutter CMOS image sensors (CISs) are widely used [1]–[3]. However, the distortion of moving subjects remains an unresolved problem, regardless of the speed at which these sensors are operated. It has been reported adopting an in-pixel analog memory (MEM) for pixels makes it possible to achieve a global shutter (GS) by simultaneously saving all of the pixels as stored charges [4]–[12]. However, because the signals from a storage unit are read in a column-wise sequence, a light shielding structure is required for the MEM to suppress the influence of parasitic light during the reading period. Pixel-parallel analog-to-digital converters (ADCs) have been reported as methods of implementing the GS in a circuit [13], [14]. However, these techniques have not been successful in operations involving megapixels because they do not address issues such as the timing constraint for reading and writing a digital signal to and from an ADC in a pixel because of the increases in the number of pixels and total power consumption of massively parallel comparators (CMs).

We previously reported a prototype of a stacked back-illuminated CIS with a 1.46-megapixel 14-bit ADC [15], [16]. In another paper, we described a Cu–Cu connection that used a wafer-to-wafer bonding technique [17]. We adopted these technologies for massively parallel pixel-wise connections. In this paper, we unveil the contact number and the contact pitch for the pixel parallel ADC. Implementing a positive feedback (PFB) circuit in the CM allows the current during operation to remain in a subthreshold region of 7.74 nA. Moreover, using a repeater circuit in which a flip flop (FF) is connected in successive stages, the design constraints on the propagation delay, which extends to the drivers of the conventional method [13], [14], pixels, and reading circuit, are reduced to only the propagation delay between FFs and the reading of the 15-bit signal of the 408 repeater columns in parallel at 148.5 MHz.

## 2. Circuit Configuration and Operation

Fig. 1 shows a simplified block diagram of this prototype. It consists of a pixel wafer on which light is incident from the back and a logic wafer that performs signal processing. The pixel

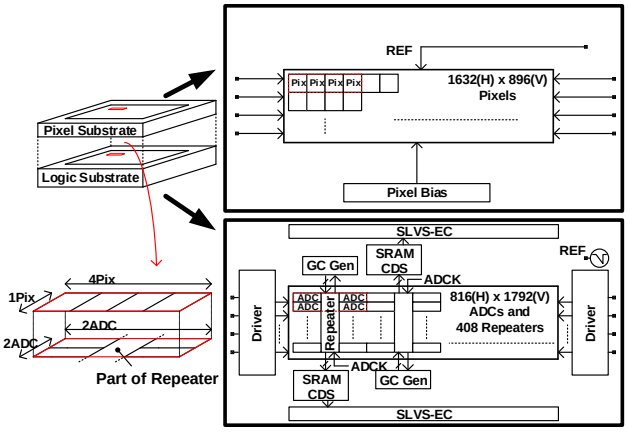


Fig.1. Simplified block diagram of pixel-parallel ADC

wafer consists of $1632^{H} \times 896^{V}$ pixels. The size of a single pixel is 6.9 μm × 6.9 μm. It contains a portion of the CM, along with a bias circuit that generates current (Icm). On the logic wafer, a portion of the CM and a 15-bit latch for digital memory are arranged in each ADC, and there are 408 repeaters that write and read gray codes (GCs) in the vertical direction for each column. In addition, the wafer is equipped with one frame SRAM for CDS and scalable low-voltage signaling with an embedded clock (SLVS-EC) for north and south I/Os. A vertical driver to drive the logic block, global driver to drive the pixel block, and digital-to-analog converter (DAC) to generate a slope voltage are also implemented.

Fig. 2 shows a simplified schematic of the pixel-parallel ADC and repeater. A portion of the CM contains differential configurations, i.e., AMP-Tr, which is the gate connected to the floating diffusion (FD); REF-Tr; BIAS-Tr for generating a bias current; TG-Tr for the transfer; and OFG-Tr for discharging photo-electrons. A pixel is reset by RST-Tr, and the fixed pattern noise (FPN) for each pixel and comparator is stored in the FD with the reset kT/C noise. A portion of the CM of the pixel is connected to a PMOS current mirror of the logic wafer and functions as a CM. The short signal return path and differential structure of the CM have immunity from common-mode noise. Because the power supply voltage of the CM

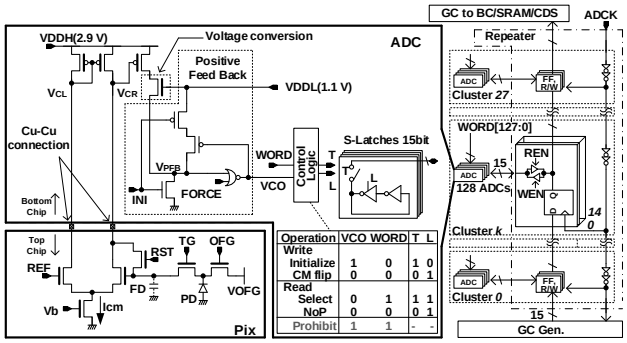


Fig. 2. Simplified circuit schematic of pixel-parallel ADC and block diagram of repeater

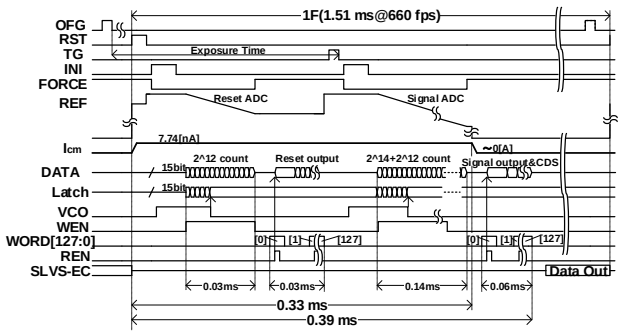


Fig. 3. One-frame timing diagram of pixel-parallel ADC

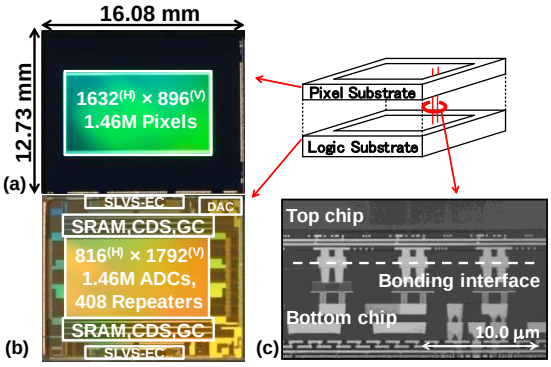


Fig. 4. Chip micrograph and part of cross section. (a) Pixel chip. (b) Logic chip. (c) Cross section of Cu-Cu bonding

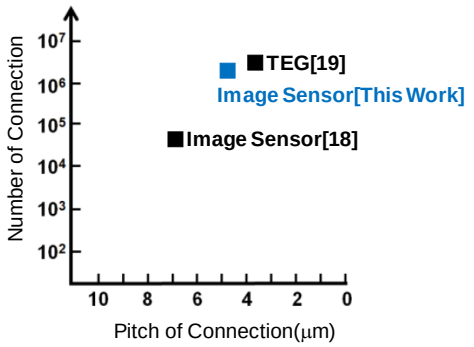


Fig. 5. Benchmark about Cu–Cu connection

affects the initial FD voltage of the pixel, it is set to 2.9 V to ensure a dynamic range. The first stage output node (VCR) of the CM is connected to the high-voltage PMOS, and its drain is connected to one NMOS Tr, with the gate connected to the logic power supply (1.1 V) to limit voltage swing. This helps to reduce the circuit area because all the subsequent circuits can use the low-voltage Tr. PFB is applied to the floating node (VPFB) of the succeeding CM. The floating node is charged at low speed by the subthreshold current of the high-voltage PMOS during the analog-to-digital (AD) conversion. It is charged more rapidly when positive feedback is applied to the low-voltage PMOS connected to the VDDL after the threshold of the NAND circuit is exceeded, which leads to a high-speed transition. A high PVT tolerance is achieved using a static latch instead of DRAM [13][14] for the signal storage element in a later stage of the CM.

The GC writing and reading operations to the latch are performed by a repeater. The repeater consists of cascaded 28-stage 15-bit FFs, which belong to clusters. A cluster is formed by 15-bit FFs with 128 pixels. The code to the latch is supplied using a digital bucket relay (DBR). The GC generated on the side opposite to the ADCK is input to the repeater via the FF. The GC has a timing error tolerance because the signal transmitted at 1 ADCK is 1 bit, and a constant power supply fluctuation is maintained during the operation. Starting from the side closer to the GC and moving to the output, 1 LSB is shifted per cluster, with a maximum of 27 LSBs for 28 stages, to form the FPN in this configuration. However, this FPN is canceled along with the reset noise and other circuit FPN in the CDS.

The timing waveform is shown in Fig. 3. First, the DAC is set to the initial voltage, and the CM is reset using the RST. The PFB part is initialized by controlling INI, and writing is enabled by WEN. Then, the slope begins. ADCK is supplied to the repeater, and data are written to the latch. The 15-bit GC is transferred using the DBR of the repeater. When the slope voltage of the FD and DAC reach the same potential, the CM flips, and the GC of the reset level is stored in the latch by terminating the writing of the GC. To suppress the collision due to the CM not flipping when the signal is read, the CM is flipped by controlling the FORCE at the end of the slope. By controlling the WORD [127:0] and REN, the data of each latch are read using the repeater, and the signal is stored in SRAM as a reset signal after conversion from the GC to binary code (BC). TG-Tr is driven to transfer the charge of the PD to the FD, and similar processing is performed to obtain the signal level. The CM is flipped with the voltage corresponding to the photo signal level, and the GC is stored in the latch. Likewise, data are output to CDS circuit using the repeater. CDS is performed on the reset BC that is read from the SRAM during the conversion of the signal from GC to BC. The calculated BC is written back into the SRAM as 14-bit BC. Then, this 14-bit BC is output to the outside of the CHIP using the SLVS-EC interface.

By setting the DAC to a low voltage when no AD conversion is being performed, the current of the CM can be turned off, which reduces the average power consumption. As a result, the time average of the 7.74 nA operation current while active is 1.67 nA at 660 fps.

## 3. Implementation Results

Fig. 4 shows the pixel chip, logic chip, and cross-section of the bonding interface of the prototype image-sensor. The pixel chip was fabricated using 90 nm 1-poly-Si 4-metal-layer CIS process technology. The pixel pitch is 6.9 μm, and there are $1632^{H} \times 896^{V}$ back-illuminated pixels. The pixel and logic chips are connected using two Cu–Cu connections per pixel. The logic chip is connected by a total of approximately 3M Cu–Cu connections, including connections between the pixel array portion, surrounding circuitry, ground lines, and other power supplies. The device was fabricated using a 65 nm 1-poly-Si 7-metal-layer logic process. An ADC with a total of $816^{H} \times 1792^{V}$ elements (i.e., twice the original pixel size in the horizontal direction and half the original size in the vertical direction) is

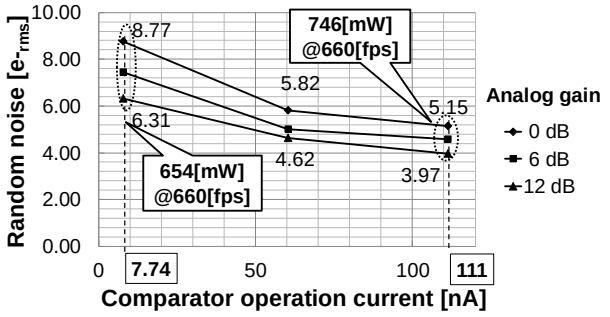


Fig. 6. Random noise versus comparator current

implemented on the logic chip. A portion of the ADC region is occupied by the repeater area, which consists of a 28-stage cascade connected cluster. The prototype chip contains 408 columns of repeaters. Eight channels, which each have 4.752 Gbps/ch SLVS-EC, are implemented on the north and south sides of the chip, for a total of 16 channels.

As shown in Fig. 5, the Cu–Cu connection for the image sensor achieves a finer pitch and larger scale connections compared with those in reference studies [18], [19].

## 4. Experimental Results

Fig. 6 shows the RN and total current vs. the CM current for a variety of analog gains. The analog gain is controlled by the REF slope. A steep slope is used for a low gain, and a shallower slope is used for a high gain. The 12-dB gain uses a 4× shallower ramp than that in the 0-dB case. The evaluation results demonstrate that it is possible for the proposed pixel-parallel ADC to control the amount of noise with the CM current and switch between the 8.77e-rms low-power-consumption mode at 654 mW and 5.15e-rms low-noise mode at 746 mW. We observe that for the same operating current, when the applied analog gain is increased, the RN decreases.

Table I summarizes the characteristics of the prototype chip. We use 2.9 V as the pixel power supply for the CM, VOFD, DAC, and drivers for the pixel control signals. A voltage of 1.1 V is used for the logic power supply of the downstream circuit. The pixel conversion gain is 60 μV/e-, and the saturation signal is 16.6 ke-. The saturation signal of this prototype is not limited by the full well capacity of PD or FD, but it is limited by the DAC dynamic range of 1 V at the full scale after CDS. The key image-sensor characteristics were achieved, including a DNL of ±0.29 LSB, an INL of -0.64%, and an FPN of 0.57 LSBrms. PLS is defined as the ratio of the FD sensitivity to the PD sensitivity and has a value of -75-dB. In a GS using an in-pixel analog MEM retention method [10–12], the MEM is exposed to light until the end of the reading row. However, the in-pixel ADC is only affected by the FD retention time during AD conversion, which is usually much shorter than the maximum MEM retention time of an image sensor with column-parallel ADC.

Table II uses two types of figures-of-merit (FoM1 and FoM2) and provides a comparison of the power, noise, dynamic range, and AD resolution performance for a rolling-shutter-type image sensor [2, 3], a MEM-storage-type GS image sensor [11, 12], and an image sensor that realizes a GS with a pixel-parallel ADC [13, 14]. A comparison of the first GS function to that in [13], which was realized using a pixel-parallel ADC, shows that we improved the FoM2 by approximately two orders of magnitude. In addition, even compared to a MEM storage GS [12] and an ADC that achieves optimal values with a rolling-

**TABLE I**
**CHIP CHARACTERISTICS**

| Item | Data | |
|---|---|---|
| Process | CIS wafer: 90nm 1 Poly 4 Metal Layer<br>Logic wafer: 65nm 1 Poly 7 Metal Layer | |
| Supply Voltage | 2.9 V / 1.1 V | |
| Num. of pixels | $1632^{(H)}$ x $896^{(V)}$ | |
| Pixel size | 6.9 μm x 6.9 μm | |
| Output interface | 16ch x 4.752Gbps/ch SLVS-EC | |
| Max frame rate | 660 fps | |
| Saturation signal | 16.6 ke- | |
| Sensitivity | 61,500 e-/lx・s<br>(green pixel, 3200K light with IR cut filter) | |
| DNL | ± 0.29 LSB | |
| INL | -0.64% | |
| FPN@ 0dB | 0.57 $LSB_{rms}$ | |
| PLS | -75 dB | |
| Conversion gain | 60 μV/e- | |
| Comparator operation current | 7.74 nA | 111 nA |
| Comparator current (time average @660 fps) | 1.67 nA | 23.9 nA |
| Power consumption | 654 mW | 746 mW |
| Rms random noise @Analog Gain 0 dB | 8.77 $e-_{rms}$ | 5.15 $e-_{rms}$ |
| Dynamic range | 65.7 dB | 70.2 dB |
| ADC resolution | 14 bit | |


F2.8, 7300lx, Exposure time = 0.56 ms, γ = 1.0

Fig. 7. Image captured at bias current of 7.74 nA/CM

shutter-type image sensor [2], this work yields the best performance index values, with a CM bias current Icm = 111 nA.

Fig. 7 shows an example of an image obtained using a current of 7.74 nA, which is the lowest CM operating current available in this prototype image sensor. The image was successfully captured with a total of approximately 3M connections consisting of two Cu–Cu connections per pixel, the subthreshold current operation with PFB, and the DBR data transfer method using repeaters. Because of the CDS, there was no effect on the image as a result of the pixel/ADC having FPN caused by subthreshold swing deviation, threshold voltage deviation, transistor size mismatch, operation current deviation, propagation delay of the CM internal circuit, cluster temporal position dependent systematic offset, asymmetricity between the 1 × 4 pixels and 2 × 2 ADCs, and REF slope delay.

## 5. Conclusion

We fabricated a 1.46 MP CIS prototype with a pixel-parallel ADC that had 14-bit performance. We realized a back-illuminated GS image sensor using approximately 3M Cu–Cu connections and a stacked structure. We reduced the power consumption by introducing a subthreshold current operation for the CM and a positive-feedback circuit. This sensor achieved the best FoM2 than the previously reported image sensors. Furthermore, the power consumption of the chip was dominated by that of the logic circuit. Thus, a further power consumption reduction could be realized by introducing power-saving technology such as clock gating and process evolution. Additional improvements in the device characteristics are possible by advancements in circuit design, noise analysis, and the appropriate handling of pixel saturation signals limited by

**TABLE II**
**PERFORMANCE COMPARISON TABLE**

| Paper | IISW2015 [2] | ISSCC2015 [3] | JSSC2017 [11] | ISSCC2017 [12] | JSSC2001 [13] | VLSI2016 [14] | **This Work** | |
|---|---|---|---|---|---|---|---|---|
| ADC | 2-Cyclic Column | Single Slope Multi Column | Multi Slope Column | Single Slope Column | Single Slope Pixel | Single Slope Pixel | Single Slope Pixel | |
| GS | N/A (Rolling) | | In pixel MEM | | **In pixel ADC** | | | |
| Pixel size [$\mu m^2$] | 3.2 | **1.43** | 5.86 | 3.4 | 9.4 | 6.6 | 6.9 | 6.9 |
| ADC resolution [bit] | **14** | 12 | ** **14** | 12 | 8 | 12 | **14** | **14** |
| Frame rate [fps] | 120 | 30 | 480 | 120 | **10000** | 120 | 660 | 660 |
| V pixels | **4320** | 3934 | 2160 | 2054 | 288 | 480 | 896 | 896 |
| H pixels | **7680** | 5226 | 3840 | 2592 | 352 | 644 | 1632 | 1632 |
| Total pixels [Mpixels] | **33.18** | 20.56 | 8.29 | 5.32 | 0.10 | 0.31 | 1.46 | 1.46 |
| Random noise [$e^-_{rms}$] | 5.2 | * **1.3** | 4.62 | 1.8 | † 115 | N/A | 8.77 | 5.15 |
| Satulation [e-] | 15300 | 9700 | 30450 | 8100 | 76336 | **220000** | 16600 | 16600 |
| Analog Gain [A.U.] | 3.5 | * 22.4 | 1 | *** 1 | 1 | N/A | 1 | 1 |
| Power consumption [mW] | 3200 | 532 | 5230 | 450 | **50** | N/A | 654 | 746 |
| Comparator operation current [nA] | N/A | N/A | N/A | N/A | †† 164.40 | N/A | **7.74** | **111.00** |
| FoM1 [$e^-_{rms}$・nJ/DRU] | 4.97 | 3.36 | **0.92** | **0.28** | 8.47 | N/A | 3.14 | 1.24 |
| FoM2 [$e^-_{rms}$・nJ/step] | **0.26** | 0.27 | 0.37 | 0.31 | 22.06 | N/A | 0.36 | **0.24** |

**FoM1=(power × noise)/(num. of pixels × fps × DRU);DRU={(saturation/gain)/noise}**
**FoM2=(power × noise)/{num. of pixels × fps × 2^(ADC resolution)}**

*** parallel multiple sampling mode**
**** 12bit 0-12dB multi slope mode**
***** It is not shown clearly in [12]**
**† 1.0[V] / 13.1[uV/e-] × 0.15%**
**†† 30[mW] / 1.8[V] / (352 × 288)**

the DAC dynamic range.

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