RTS noise characterization and suppression for advanced CMOS image sensors

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Abstract The transistor noise is becoming more important in ultralow noise CMOS image sensors as well as with 3D stacking structures. This paper presents statistical measurement results and analyses of random telegraph signal noise of source follower transistors using array test circuits. The impacts of driving current as well as the shape of transistor gate are investigated and discussed toward the suppression of random telegraph signal noise. In addition, parameters to detect and analyze the impacts of random telegraph signal noise is discussed in detail.

Keywords: random telegraph signal noise, source follower transistors, CMOS image sensor

1. Introduction

Random telegraph signal (RTS) in current-voltage characteristics of MOSFETs occurs due to the capture and emission of a channel carrier(s) by a gate insulator trap(s) [1]. RTS noise (RTN) in CMOS image sensors is becoming more important as being a major noise source in low noise CMOS image sensors [2-3]. RTN of in-pixel source follower (SF) has been considered to be the important as it is difficult to be reduced by circuit technologies [4]. Meanwhile, 3D stacking technologies of light receiving substrate and logic circuit substrate(s) have been driving force of development in CMOS image sensors in recent years for performance improvement as well as adding new function [5-9]. The electrical connection pitch has been rapidly scaled, CMOS image sensors with the pixel-wise connections were reported to be useful for integrating pixel- or pixel block-wise circuitry such as analog-to-digital converters [7-8]. In this case however, highly-scaled transistors in the bottom substrate are to be used for analog front-end circuits such as comparators [7-8], or even in-pixel SF driver [9]. Consequently, measurement and characterization of RTN in large number of transistors are critically important for noise suppression of advanced CMOS image sensors.

We have been researching on statistical measurements and analyses of large number of transistors using array test circuits with fast measurement speed and high precision, and shed light on the impacts of transistor structure, process conditions, operation conditions and so on [10-13]. In this presentation, the recent advancements of our research activities are summarized.

2. Measurement results and discussions

2.1 Effect of operation current

Fig.1 and 2 show a circuit schematic of the array test circuit and a chip micrograph used in this work. The chip was fabricated by a 0.18μm 1-poly-Si 5-metal layer CMOS image sensor technology with 3.3V supply voltage. The pixel pitch was 10μm. The circuit structure is quite simple so that process conditions can be modified easily. The chip outputs analog signal. Fig.3 shows the analog front-end circuit board of the measurement system. The system background noise is as low as 60μmV_{rms} [13].

Fig.4 shows the measured distribution of RTN by means of (a) root mean square of output voltage (V_{rms}) and (b) amplitude of signal transitions for different current conditions, respectively. It is obvious that with a lower operation current, the appearance probability is smaller, however the impact of a trap toward the amplitude becomes larger. Fig. 5 illustrates the mechanism to explain the obtained behavior [14].

2.2 Effect of transistor gate shape

Fig.6 shows the illustrations of octagonal and trapezoidal shaped transistors measured with conventional rectangular transistors [15]. Fig.7 shows the measured distribution of V_{rms} for (a) rectangular and octagonal shaped buried channel SF and (b) rectangular and trapezoidal shaped surface channel SF with various gate width, respectively. It is obvious that octagonal transistor without shallow trench isolation (STI) edge results in lower noise. Also, under the same gate length of 0.44μm, distribution of RTN seems to be governed by gate width at source electrode side of transistors.

2.3 Effect of time constants and number of states

Fig.8 and 9 shows the measurement results of transistors with gate width/length of 0.28μm/0.22μm, respectively, where Fig.8 shows typical waveforms of RTN and Fig.9 shows the relationship between (a) V_{rms} and (b) RTN amplitude with correlated double sampling (CDS) and without CDS, respectively [16]. The values of V_{rms} with and without CDS are very different depending on the time constants and number of states, whereas the values of amplitude with and without CDS are highly correlated. The results suggest that the amplitude should be another important parameter to detect and characterize the RTN in addition to V_{rms}.

4. Conclusion

The recent advancement of measurements and analyses of RTN using array test circuits were summarized. The proposed methodologies and findings are important for development of advanced CMOS image sensors.

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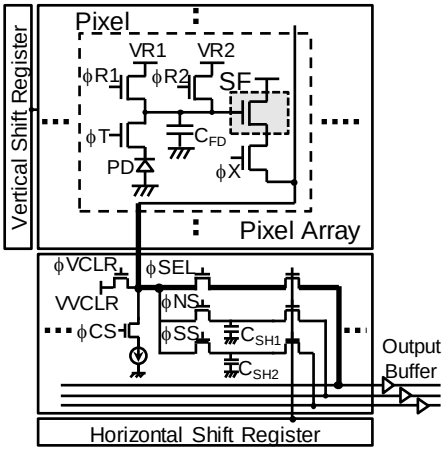

Fig. 1. Circuit schematic of array test circuit for characterization of RTN used in this work.

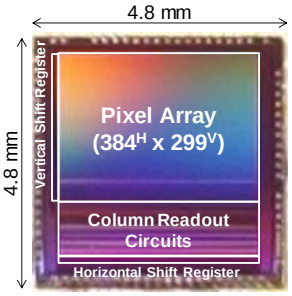

Fig. 2. Chip micrograph of the array test circuit.

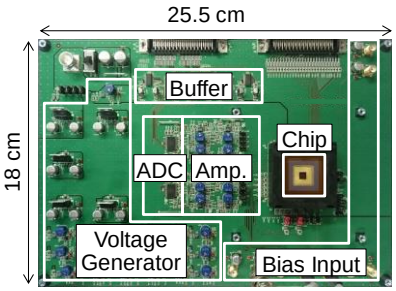

Fig. 3. Picture of circuit board used in the measurement system.

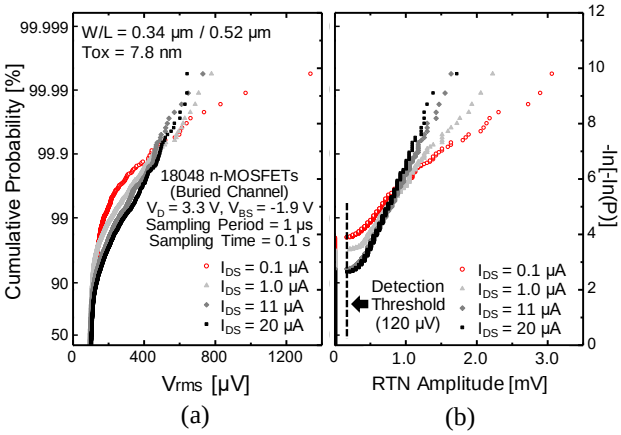

Fig. 4. Distribution of RTN by means of (a) root mean square of output voltage and (b) amplitude for different current conditions, respectively.

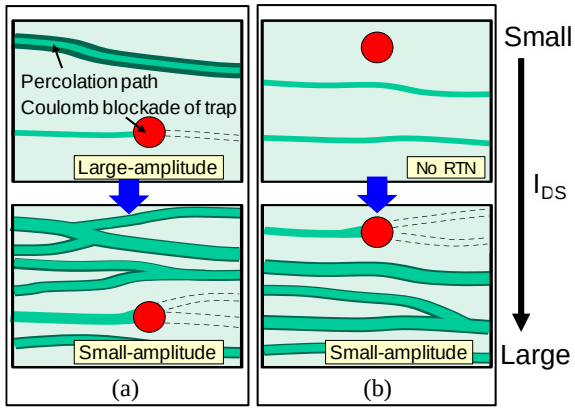

Fig. 5. Schematic diagram of channel percolation and interaction of trap illustrating a proposed model to explain the obtained RTN behavior toward current density.

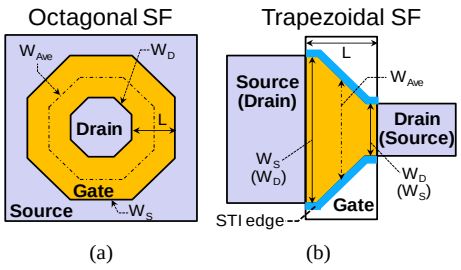

Fig. 6. Schematic illustrations of (a) octagonal and (b) trapezoidal gate structures measured in this work.

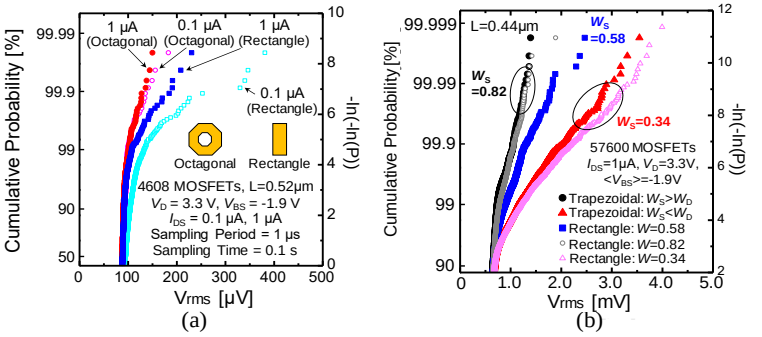

Fig. 7. Distribution of V_{rms} for (a) rectangular and octagonal shaped buried channel SF and (b) rectangular and trapezoidal shaped surface channel SF with various gate width, respectively.

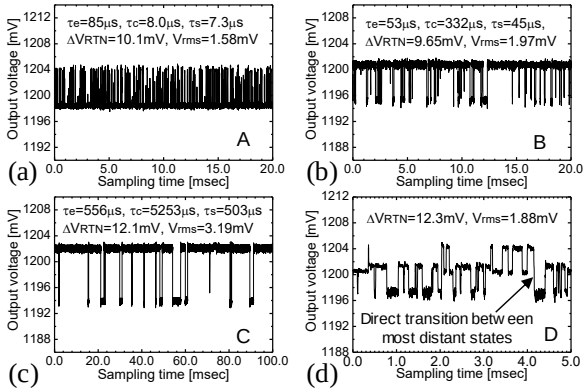

Fig. 8. Typical waveforms of RTN with various time constants, amplitude, and number of states.

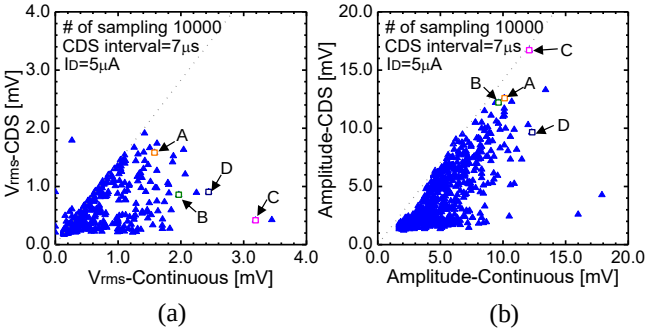

Fig. 9. Relationship between (a) V_{rms} and (b) RTN amplitude with correlated double sampling (CDS) and without CDS, respectively.