On a BSI Image Signal Accumulation Sensor of 100 Mfps

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Abstract We developed a test sensor of an ultra-high-speed image signal accumulation sensor (ISAS). The target frame rate and frame count were respectively 50 Mfps and 1,220 frames with the image signal accumulation function for repetition of image capturing. For image signal accumulation, 4-phase folded and looped CCDs are used as in-pixel signal storage. For the ultra-high-speed, the multi-collection-gate structure is incorporated. The number of collection gates is four. The 4-phase CCDs and 4-collection-gate structure perfectly worked for pipeline signal recording. This paper presents an ISAS modified based on the evaluation of the test sensor. To double the frame rate to 100 Mfps, the pixel size is reduced from 72.56 um to 57.6 um, sacrificing the pixel count to about the half, 600, and the p-well is redesigned to increase the horizontal field over the p-well for a higher travelling velocity of signal electrons.

Keywords: Ultra-high-speed, image signal accumulation sensor, multi-collection-gate

1. Introduction

Our sensor is designed based on two operation concepts: Backside-illuminated multi-collection-gate (BSI MCG) image sensor [1] and image signal accumulation sensor (ISAS) [2].

1.1 Backside-illuminated Multi-collection-gate

To fully acquire image signals in low-light condition, the BSI structure is used to increase the fill factor up to 100%. Four collection gates are applied at the front side in order to collect the signal charges generated at the light conversion layer. Fig. 1a) shows the cross-section of the BSI structure of one pixel.

1.2 Image signal accumulation sensor

The ISAS accumulates a large number of charge packets by continuously capturing pictures. The loop is created by connecting the last CCD element to the first element. Each collection gate is connected to CCD elements for each quadrant. The layout of ISAS is shown in Fig. 1b).

The ISAS works in two modes:

- *Continuous overwriting:* The overwriting gate is high so that old signals drain out. In this mode, the newest signals are successively stored in the CCD storage.
- *Signal accumulation:* The overwriting gate is low so that the latest image signals are added to the previous ones.

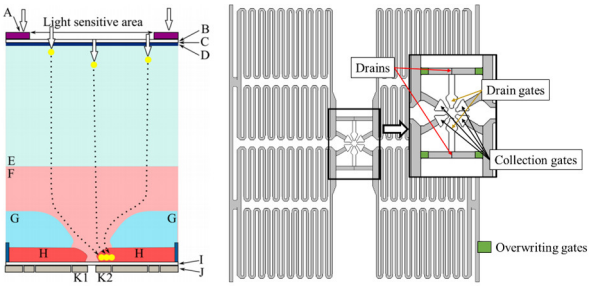

Fig. 1. a) Cross-section of the BSI MCG image sensor, b) the layout of the ISAS sensor

2. Operation concept

By combining two aforementioned concepts, we developed Backside Illuminated Multi-Collection-Gate Image Signal Accumulation Sensor [3]. The pipeline operation is described in Fig. 2. The first charge packet shown in Fig. 2a) is collected at CG1. Then, charges are transferred to CCD memory at the same time with the second charge packet collected at CG2, shown in Fig. 2b). Similarly, CG3 and CG4 will work in turn and transfer the charge packets to CCD memories, as shown in Fig. 2c) and 2d). Then, the sensor repeats the process for the fifth and next charge packets, shown in Fig 2.e) and f).

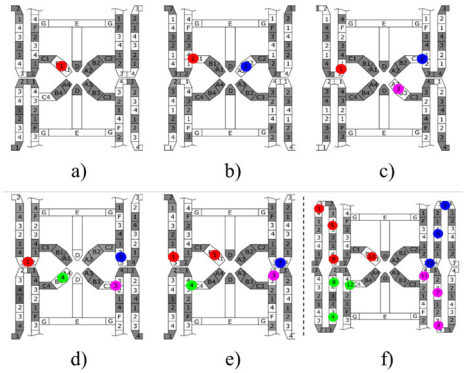

Fig. 2. The pipeline operation of BSI MCG ISAS [3]

3. P-well design and arrival time distribution

The temporal resolution of the image sensor is defined by the standard deviation of the electron's arrival time from backside to frontside [4]. To reduce the average arrival time, p-well masks are implanted to the sensor. Moreover, the function of p-well is crucial to prevent signal electrons migrating directly to the CCD memories.

In this sensor, the p-well design consists of three masks that creates a linear E-field (shown in Fig. 3a)):

a) Mask 1 (yellow): The first mask covers whole pixel except the central area. The implantation energy is low.
b) Mask 2 (green): The second mask is a comb-like shape with many straight twigs toward to the center
c) Mask 3 (blue): The third mask covers only the pixel boundary. The implantation energy is the highest value that the manufacturer provides.

The 3D potential created by three p-well masks is visualized in Fig 3b). Due to the high energy doped in p-well 3, the width is as thin as possible to reduce the horizontal E-field at the pixel boundary. This field is to prevent the spatial crosstalk and assist electrons to travel to the center faster. In Fig 3c), the cross section of the 3D potential along the pixel's diagonal shows the linearized potential profile. The slighter field near pixel boundary is affected

by deep p-well mask 3, while the field at the central area is due to the transient potential to the center hole. The slope in the middle area is 0.027 V/µm.

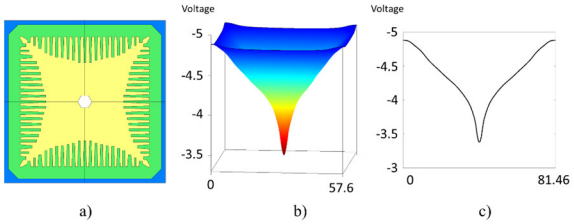

Fig. 3. a) three p-well masks, b) 3D potential created by p-well, c) cross-section of potential created by p-well

Fig. 4 demonstrates the electron path from the backside to the collection gate. The red curve and blue curve are the electrons' trajectories with and without random motion, respectively. By the linearized field designed by p-well masks, charges can easily move from the boundary to the central area in a very short time.

For example, from the point x=5.52 µm, y=52.08 µm, z=25.2 µm to the collection gate, the mean and standard deviation of electron travel time using Monte Carlo (MC) simulation are 8.02 ns and 2.00 ns, respectively. The travel time without random motion calculated by a device simulator, SPECTRA, is 8.19 ns.

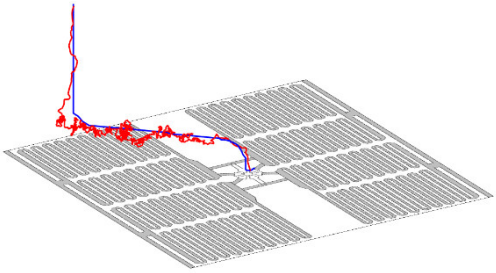

Fig. 4. The trajectories of electrons in red and blue with and without random motions, respectively

By using MC simulation, the time distribution and temporal resolution are calculated. The average time (µ), standard deviation (σ), temporal resolution (Δt=2σ), and the 95th percentile (t_{95}) for various fill factors – 100%, 75%, 50%, 25%, and 10% are listed in Table 1.

Table 1. Parameters on the electron arrival time distribution

Fill factor	100%	75%	50%	25%	10%
µ (ns)	4.37	3.97	3.06	2.07	1.28
σ (ns)	2.44	2.19	1.74	1.13	0.61
Δt (ns)	4.88	4.39	3.48	2.25	1.23
t_{95} (ns)	8.82	7.84	6.31	4.07	2.35
t_{95}/Δt	1.81	1.79	1.82	1.81	1.92

For the fill factor of 100%, t_{95} is 8.82 ns, so the framerate is 113 Mfps.

4. Design of folded channels

In order to transfer the electron in the loop, the folded structure is utilized to change the flow directions of electrons. The width of channel must be carefully adjusted depending on the p-well masks. In Fig. 5a), a bend located in p-well mask 1 and p-well mask 2 are chosen to evaluate the voltage differences. The flat potential along the path is shown in Fig. 5b). The blue and green curves are the potential in case of only p-well mask 1 (PW1) and both p-well mask 1 and p-well mask 2 (PW1+PW2), respectively. The red curve is the mixing area that contain p-well mask 1 and a part of p-well mask 2. The peak-to-peak voltages in case of PW1, PW1+PW2, and mixing area are 0.050 V, 0.069 V, and 0.066 V, respectively.

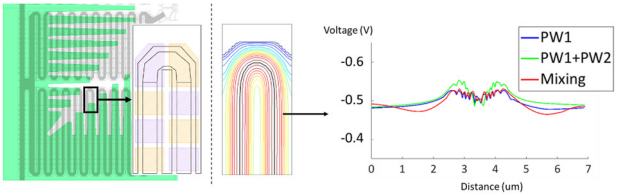

Fig 5. a) The design of a bend, b) the potential along the channel in different masks

The 4-phase transfer scheme is applied to the CCD elements as shown in Fig. 6a). V1 and V2, V2 and V3, and V3 and V4 are applied high voltages alternately, so the charge packet will be transferred from left to right at a bend as shown in Fig. 6b). The maximum charge handling capacity (Qmax) and highest local electric field (E-field) in areas A, B, and C are listed in Table 2.

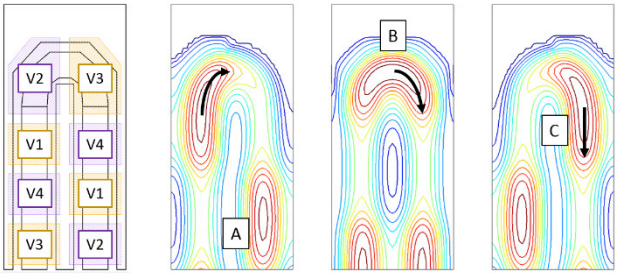

Fig. 6. Potential profile when apply 4-phase transfer scheme

Table 2. The Qmax and E-field at a bend

Area	Qmax (Electrons)	E-field (V/µm)
A	3222	9.217
B	4842	10.780
C	3987	10.182

5. Conclusion

In this paper, we summarize the concept and improvements of Backside-illuminated Multi-collection-gate Image Signal Accumulation Sensor. The highest frame rate that the sensor can achieve is 113 Mfps.

References

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