[Poster Presentation]

A Current-Mode Differential Sensing CMOS Imager for Optical Linear Encoder

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Abstract This paper presents a high speed low noise CMOS imager for optical linear encoder. Dual sensor arrays and the corresponding readout circuit are implemented for incremental and absolute signals, respectively. For incremental signal, current-mode differential sensing (CMDS) frontend with buffered direct injection (BDI) is proposed for DC background cancellation and high response bandwidth. Transimpedance amplifier (TIA) is implemented for current-to-voltage conversion with low-pass filtering function for noise reduction. Programmable amplifier (PGA) is implemented for single-to-differential conversion and full-range fitting for the following 12-bit SAR analog-to-digital converter (ADC). For absolute signal, 42 sensor pixels with the corresponding dual-threshold quantizer and latch are implemented. This work achieves a SNR of 63.4dB, a phase error of 33.8 degree at 3.3MHz incremental input, and an ADC ENOB of 11.08-bit at a sampling rate of 200kHz.

Keywords：optical encoder, transimpedance amplifier, position detection.

1. INTRODUCTION

The applications of precise measurement and positioning devices are widely used in the manufacture processing and testing equipment. Linear encoder is commonly used to detect the position and displacement of the moving mechanical part. Linear encoders can be realized with many different physical properties in order to encode position information including optical, magnetic, capacitive, inductive and so on. Optical linear encoder is the most accurate solution and dominates the high resolution applications.

Fig. 1 shows the optical linear encoder system, which is composed of light source, condenser, scale (absolute code and incremental grating), and photo detector. In the absolute encoder, every absolute code corresponds to a coarse position of the objects. The precise information of the position can be obtained by interpolating the sinusoidal output signal of incremental encoder. When the position of scale is moving, four incremental sinusoidal signals are generated with a 90° shift between each other, and the quadrature light signals are converted into currents by photodetectors. However, since the DC level of signals is much higher than the AC signals, direct current-to-voltage conversion using transimpedance amplifier (TIA) [1] may cause output saturation and signal clip. Differential readout of the quadrature signals (I0°-I180° & I90°-I270°) are usually implemented to cancel out the background and common-mode noise. In Conventional readout approach [2], TIA is used for I-to-V conversion and instrumentational amplifier (IA) for differential operation. The I-to-V gain of TIAs is limited by DC signal level to avoid the signal saturation, which suffers the achievable signal-to-noise ratio (SNR). Moreover, the required multiple high-performance opamps consume huge power with worse noise and phase delay due to the cascaded stages. Although the differential TIA frontend [3] can subtract two opposite currents, the response bandwidth is limited by the large capacitance of photodiodes.

This paper presents a current-mode differential sensing (CMDS) frontend with background and common-mode noise cancellation for incremental encoding signal readout. For absolute encoding signal readout, 42 sensors with the corresponding readout path and dual-threshold quantizer are implemented for a 42-bit output. The rest of this paper is organized as follows. Section II describes the architecture and details of proposed design. Section III presents the simulation results. Section IV gives the conclusion.

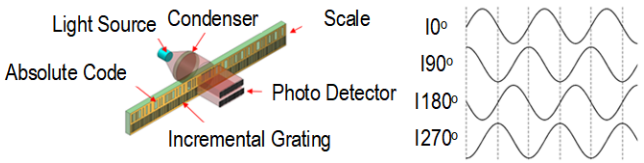

Fig. 1. Optical linear encoder system and 4 phases of input signals.

2. OPTICAL LINEAR ENCODER ARCHITECTURE

Fig. 2 shows the block diagram of the proposed CMDS frontend composed of buffered-direct injection (BDI), common-mode current cancellation, TIA, programmable gain amplifier (PGA), and analog-to-digital converter (ADC). The BDI technique [4] is adopted to block the sensor parasitic capacitance for a high-bandwidth response. The differential operation is implemented in current-domain to achieve DC signal cancellation before TIA. The differential current signal is then processed by the following TIA, low-pass filter, programmable gain amplifier (PGA), and finally quantized by a 12-bit SAR ADC.

A. Incremental Encoder Readout Circuit

For incremental encoding signal readout, the BDI technique composed of common-source amplifier and injection device is applied to block the photodiodes capacitance from the input of the TIA. With the negative feedback loop of BDI, the biasing voltage across the photodiode is locked at a relatively constant value, which effectively reduces the effective capacitance of photodiodes. In this work, the equivalent capacitance is reduced by $A_{CS}g_{m1}r_{o1}$, where A_{CS} is the gain of the common-source amplifier, g_{m1} and r_{o1} are the transconductance and output impedance of M1, respectively.

The buffered injected currents from sensing diodes with 180° shift are mirrored and subtracted by each other in current domain to achieve the common-mode current cancellation. The differential output current, Iout, is then fed into the input of TIA for I-to-V conversion. The additional noise and phase

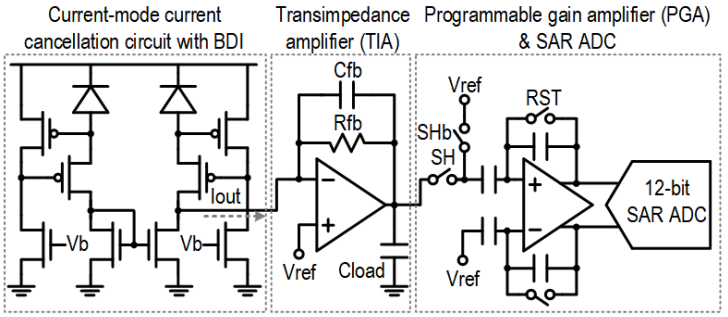

Fig. 2 Readout circuit of incremental encoder.

Table. I

Rfb	125kΩ
Cfb	150fF
Cload	1.8pF
SNR	63.4dB
Phase delay@ 3.3MHz	33.8°

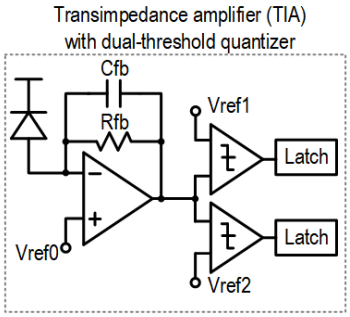

Fig. 3 Readout circuit of absolute encoder

delay from current mirrors are carefully minimized to meet the system requirement. The feedback resistance Rfb, feedback capacitance Cfb, and loading capacitance Cload need to be selected well for the trade-off between phase shift and noise performance. The choice of Rfb and Cload depends on the required I-to-V gain and noise performance with a tradeoff of phase shift. To achieve the target SNR>60dB and phase shift<35° at 3.3MHz incremental signal, the optimal design implementations are summarized in Table. I.

A single-to-differential programmable gain amplifier (PGA) is implemented for interfacing of TIA's output and the following SAR ADC. A 12-bit SAR ADC using monotonic capacitor switching [4] is implemented for its high energy efficiency and robustness.

B. Absolute Encoder Readout Circuit

The absolute encoder consists of 42 sensors and the corresponding readout circuit. Fig. 3 shows the readout circuit of each channel which is composed of TIA, dual-threshold quantizer, and SR latch. Due to the released linearity requirement in absolute encoding, a simple differential pair is implemented as the opamp of TIA for power reduction. The dual-threshold quantizer is implemented with two comparators and adjustable thresholds for noise margin and error correction. The outputs of 42 channels are sampled simultaneously by the SR latches and readout serially controlled by the embedded shift register.

3. SIMULATION RESULT

Fig. 4 shows chip micrograph. Fig. 5 shows the common-mode current cancellation of CMDS with a DC levels of 10μA to 90μA and a AC signal of 4μA. It shows that the input AC current I(Rfb) keeps as a constant after CMDS under varied DC levels. Fig. 6 shows the achieved ENOB of after quantization with a simulated sinusoidal current inputs at sensor nodes. With the aid of BDI, the resistance (Rfb) and capacitance (Cfb) chosen from the optimization procedure, the achieved SNR is 63.4dB and the phase delay at 3.3MHz is 33.8°. The total power consumption of the whole chip including absolute and incremental encoders is 20mW.

4. CONCLUSION

This paper presents a CMOS imager with incremental and absolute signals sensing and readout for optical linear encoder. The employed BDI technique blocks the photodiodes capacitance from the input of the TIA to increase the system response bandwidth. The proposed CMDS circuit effectively cancels out the DC signal component and common mode noise as well. The implemented TIA with the

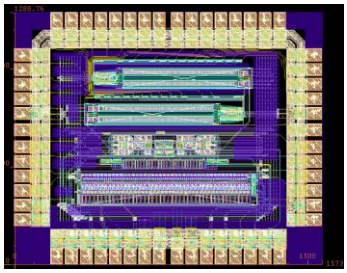

Fig. 4 Chip micrograph.

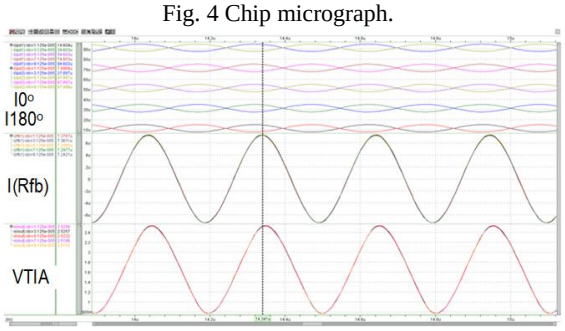

Fig. 5 Common-mode current cancellation of CMDS.

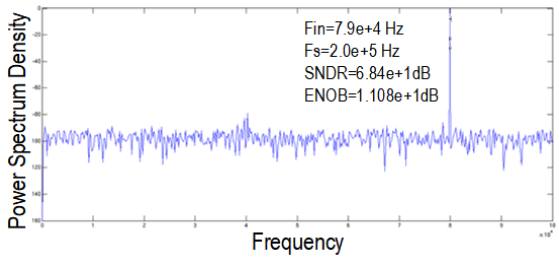

Fig. 6 FFT of the whole system

well-selected resistance and capacitance achieves the optimized SNR and phase shift tradeoff. The system phase delay at 3.3MHz is as low as 33.8° and the SNR is 63.4dB. A 12-bit SAR ADC is also implemented for incremental signal interpolation with an ENOB of 11.08 bits. A simplified TIA and dual-threshold quantizer are implemented for absolute encoder signal readout with reduced power consumption and tunable noise margin.

REFERENCES

[1] D. Maschera et al., "An automatically compensated readout channel for rotary encoder systems, " in *IEEE Transactions on Instrumentation and Measurement*, 2001.

[2] Trong-Hieu Tran et al., "The Front-End Readout as an Encoder IC for Magneto-Resistive Linear Scale Sensors." in *Sensors Journal*, 2016.

[3] C.-T Chiang et al., "Design of a CMOS phase to digital transducer for optical incremental sensors," in *Sensors and Actuators A: Physical*, 2011.

[4] C. C. Liu et al., "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," in *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731-740, April 2010.